APPLICATION

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TITLE: BACKSIDE BURIED STRAP FOR SOI DRAM TRENCH CAPACITOR

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BACKSIDE BURIED STRAP FOR SOI DRAM TRENCH CAPACITOR

TECHNICAL FIELD

The field of the invention is that of DRAM arrays on SOI wafers, in particular for ultra-thin insulating layers.

BACKGROUND OF THE INVENTION

In SOI circuits having trench capacitor DRAM arrays, the capacitor is connected to the pass transistor through a buried strap that makes electrical contact with the device layer at a vertical surface abutting the capacitor trench.

The conventional DRAM layout in which cells are staggered so that "passing wordlines" pass over trench capacitors in adjacent rows of the array works when the thickness of the insulator between the passing wordline and the capacitor is great enough to suppress coupling (including shorts), but the decreasing thickness of the device layer has caused the thickness of the trench top oxide (TTO) to decrease correspondingly, so that it is no longer possible to retain the passing wordline layout with conventional manufacturing tolerances.

Accordingly, in the prior art, the cell layout for SOI circuits with thin device layers must be changed, increasing the size of the DRAM cell.

The art would benefit from a DRAM cell structure that retains the advantages of a thin device layer while still permitting the passing wordlines to pass over the trenches in adjacent rows.

SUMMARY OF THE INVENTION

The invention relates to a DRAM cell structure for SOI technology in which the buried strap makes contact with the bottom of the device layer.

A feature of the invention is the recess of the trench center electrode to a depth within a manufacturing tolerance of the bottom of the device layer.

Another feature of the invention is an isotropic etch to expand the trench laterally to undercut the device layer with an expanded aperture.

Another feature of the invention is filling the expanded aperture with a conformal conductor.

Yet another feature of the invention is coating the surfaces of the expanded aperture with a conductive material before the filling step.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows in cross section a DRAM cell according to the invention.

Figures 2 through 6 show intermediate steps in the construction of the cell of Figure 1.

Figure 7 shows in cross section a prior art DRAM cell.

Figures 8 through 10 show corresponding steps in an alternative embodiment.

DETAILED DESCRIPTION

Referring now to Fig. 7, there is shown in cross section a portion of a prior art DRAM SOI cell. Trench 100 has been etched into substrate 10 through silicon device layer 60 (~ 35nm thick) and buried oxide (BOX) 50 (100 - 300nm thick) , illustratively to a depth of several microns. An insulator, e.g. oxide or oxide-nitride has been deposited conformally inside the trench and doped poly center electrode 105 has been deposited. At the top left of the trench, shallow trench isolation (STI) 70 separates the cell from other portions of the circuit. To the right of the trench, a portion of silicon device layer 60 has formed in it two FETs 210. The FET in the center of the Figure is connected to trench capacitor 100 through doped poly strap 211. Strap 211 is one electrode of transistor 210, diffusion 220 being the other. Gate insulator 213 and gate 212 complete transistor 210.

Diffusion 220 is shared with both cells, being in common with both transistors 210. It will be the bitline contact, making electrical contact with bitline 225, shown extending left and right to contact other cells in the array.

Gates 212 are also wordlines, extending perpendicular to the plane of the paper to make contact with other cells. On the left of the Figure, poly 232, referred to as a "passing wordline" extends to make contact with cells before and behind the plane of the paper, in a conventional folded bitline array layout. This geometrical arrangement is used so that adjacent bitlines can go to opposite sides of the sense amplifiers and thus have improved common mode noise rejection.

The problem addressed by the present invention is that the insulation between the passing wordline 232 and the center electrode is only the thin gate oxide 213', the same thickness as the gate oxide 213 of transistors 210. In current technology, the thickness of the SOI layer is so small that manufacturing tolerances in recess control do not permit filling this area with insulator.

When the thickness of the device layer becomes less than about 100nm, the manufacturing tolerances (+/- 35nm for a 100nm device layer) can combine such that the thickness allowed to fill with TTO is too thin to reliably isolate the passing wordline from the trench electrode. In that case, it is necessary to change the layout from the compact version illustrated here to a larger one that displaces the passing wordline from the trench.

Referring now to Fig. 1, there is shown the result of the inventive process, in which center electrode 105 is recessed to about midway through BOX 50 and an expanded trench aperture is formed by isotropic etching. This expanded aperture extends laterally nominally 25nm, to make contact with the bottom side (backside) of device layer 60. The trench top oxide can now be the full thickness of device layer 60, giving an ample safety margin for insulation. The following figures illustrate steps in the process.

Starting out with a standard SOI wafer having a preferred BOX thickness of about 200nm and a P-type device layer thickness of 35nm, standard pad layers are formed: e.g. thin thermal oxide, deposited nitride 80 (100 - 300nm) and CVD oxide (500 - 1000nm). The BOX thickness will vary depending on the technology used to produce the wafer. For SIMOX wafers, the BOX ranges 100 - 500nm. For bonded wafers, the BOX ranges 10 - 300nm. Deep storage trenches are etched through the SOI, BOX and into the substrate. In the course of the etching, most of the CVD oxide is consumed. Standard trench capacitor processing is performed, including a plate outdiffusion if desired, capacitor dielectric lining (e.g. oxy-nitride) deposition of (N^+) doped poly. The plate and node dielectric are omitted from the drawings for simplicity. The center electrode material 105 is recessed to a depth nominally in the midpoint of BOX 50, leaving apertures 110 to be filled with the strap and then with insulator. The result is shown in Fig. 2, in which the trench extends through pad nitride 80, SOI 60, BOX 50 and into substrate 10.

Next, an isotropic etch attacking the BOX in preference to silicon expands aperture 110 laterally to form expanded aperture 115. An odd shaped plug

of oxide 52 remains after this etching step. A requirement for this etch is that it produce a clean surface on the bottom of layer 60, suitable for making electrical contact between the buried strap and the device layer. Suitable etches are a wet etch, such as HF and an isotropic dry etch, such as a fluorine containing gas such as SF_6, NF_3, CF_4/O_2, CF_4. Standard works such as "Silicon VLSI Technology", Plummer, Deal, Griffin, pp 644 - 647, Prentice Hall, 2000 discuss the properties of various gases.

Illustratively, for a ground rule of 100nm, the expanded aperture 115 extends laterally by 25nm under device layer 60 to give a sufficiently large bottom contact area, without risk of shorting through oxide plug 52 to the adjacent aperture on the left. As ground rules change, the tolerances required for a safety margin will charge correspondingly. Note that the bottom corners of aperture 115 extend down toward substrate 10. It is a requirement on the depth of the recess and the etch process that the buried strap not be allowed to short to the substrate. The result is shown in Figure 3.

Next, strap 120 is formed by deposition of conductive poly (N^+) in aperture 115. The poly is recessed by a directional etch that does not affect the contact at the bottom surface of layer 60, leaving aperture 117 that extends slightly down below SOI layer 60. This recess serves to keep the strap diffusion away from the top surface. In addition, if the strap material is in contact with the vertical surface of the device layer, there may be diffusion from the strap that would adversely affect the transistor characteristics (i.e. short channel effects, junction leakage, etc.).

It is an advantageous feature of the invention that the depth of this recess is non-critical because the thickness of the remaining poly strap in the center does not have a significant effect on the current flow in and out of the capacitor. The result of this step is shown in Figure 4.

Next, as shown in Figure 5, a convenient material, such as CVD or HDP oxide 140, is deposited and planarized to the same level as pad nitride 80.

Photoresist 180, having aperture 182, is patterned and an etch that attacks pad nitride 80 and SOI 60 in preference to BOX 50 and oxide fill 140 cleans the poly material of the buried strap out of the area between the trenches. this step forms the isolating trenches of shallow trench isolation (STI) extending through the device layer. The expanded aperture extends before and behind the plane of the paper as well as left and right. The isolating trenches remove all of the device layer except for the active area, so that the portion of the buried straps outside the active area and the trench are trimmed. The dimensions of aperture 182 are chosen such that the strap remains only in overlap between the active area extending to the right in the Figure and the trench; i.e. all of the strap outside the trench is removed. The result is shown in Figure 6. The purpose of this step is to prevent leakage between adjacent cells through the SOI.

The area removed in the previous step is filled with oxide and planarized to form the STI between cells. Transistors are formed in the device layer to complete the cells, as shown in Figure 1. The passing wordlines 214 in Figure 1 have been shown as displaced in order to illustrate a benefit of the

invention - that the wide and thick insulator provided by this invention is very tolerant to the alignment between the trench capacitors and the passing wordlines.

Referring now to Figure 8, there is shown the result of steps in an alternative embodiment in which, before deposition of poly for the buried strap, a conductive liner 322 of metallic nitride (e.g. WN, TiN) or other low resistance material has been deposited conformally by CVD. This version has the advantage that a material can be selected that deposits more conformally and/or bonds to the SOI layer 60 better than the doped poly material of the first embodiment - i.e. that the improvement in adhesion and conductivity is worth the extra cost of this step. The thickness of layer 322 is a nominal 5nm. After this step, amorphous or poly silicon 320 is deposited as in the first embodiment.

As in Figure 5 of the first embodiment, liner 322 and poly 320 are recessed and the aperture is filled with oxide 140 and planarized. Figure 9 shows the result of the planarization step, plus the deposition and patterning of photoresist 180 with the same aperture 182 as in the first embodiment. Note in Fig. 9 that, since the liner makes contact with the bottom of SOI layer 60, an etch chemistry that attacks poly 320 in preference to liner 322 reduces the chance that the etchant will extend its attack laterally. An anisotropic etch is preferred so that the liner remains intact. Preferred etches are HBr, Cl_2, Cl_2/HBr/O_2. Other dry etches such as SF_6 or CF_4 or wet etches such as HNO_3:H_2O:HF(+CH_3COOH) may be used.

Figure 10 shows the result of cleaning out the exposed nitride pad, 80, SOI and liner and strap outside the area of the trench, then filling with oxide 170 and leaving a solid plug of dielectric 140 surrounded by the oxide 170 of the STI. Pad nitride 80 will be stripped, transistors will be formed in SOI layer 60 and interconnections will be formed to complete the circuit, as in the first embodiment.

While the invention has been described in terms of two preferred embodiments, those skilled in the art will recognize that the invention can be practiced in various versions within the spirit and scope of the following claims.